L Number	Hits	Search Text	DB	Time stamp
1	1474	ferroelectric and perovskite and (anneal or annealing or heat)	USPAT; US-PGPUB	2003/11/06 11:35
2	90	(ferroelectric and perovskite and (anneal or annealing or heat)) and (densification or (pin adj holes))	USPAT; US-PGPUB	2003/11/06 11:33
3	56	((ferroelectric and perovskite and (anneal or annealing or heat)) and (densification or (pin adj holes))) and @ad<20000417	USPAT; US-PGPUB	2003/11/06 11:34
4	101	densification and (pin adj holes)	USPAT; US-PGPUB	2003/11/06 11:33
5	0	(densification and (pin adj holes)) and ferroelectric	USPAT; US-PGPUB	2003/11/06 11:34
6	0	(densification and (pin adj holes)) and PZT	USPAT; US-PGPUB	2003/11/06 11:33
7	236	densification and ferroelectric	USPAT; US-PGPUB	2003/11/06 11:34
8	168	(densification and ferroelectric) and (anneal or annealing or heat)	USPAT; US-PGPUB	2003/11/06 11:34
9	102	((densification and ferroelectric) and (anneal or annealing or heat)) and @ad<20000417	USPAT; US-PGPUB	2003/11/06 11:34
10	1	(((densification and ferroelectric) and (anneal or annealing or heat)) and @ad<20000417) and pin	USPAT; US-PGPUB	2003/11/06 11:34
11	46	(((densification and ferroelectric) and (anneal or annealing or heat)) and @ad<20000417) and perovskite	USPAT; US-PGPUB	2003/11/06 11:35

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TITLE: Compound, high-K, gate and capacitor insulator layer

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INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kizilyalli; Isik C.	Orlando	FL	N/A	N/A
Ma; Yi	Orlando	FL	N/A	N/A
Roy; Pradip Kumar	Orlando	FL	N/A	N/A

US-CL-CURRENT: 257/310, 257/295 , 257/311 , 257/312 , 257/313 , 257/314 , 257/E21.01 , 257/E29.165

ABSTRACT:

A gate or capacitor insulator structure using a first grown oxide layer, a high-k dielectric material on the grown oxide layer, and a deposited oxide layer on the high-k dielectric material. The deposited oxide layer is preferably a densified deposited oxide layer. A conducting layer, such as a gate or capacitor plate, may overlay the densified oxide layer.

20 Claims, 2 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 1

CLAIMS:

The invention claimed is:

1. An integrated circuit having a silicon substrate with a surface, comprising: a densified grown oxide layer on the silicon substrate; a high-k dielectric layer on the densified grown oxide layer, the densified grown oxide layer reducing strain between the silicon substrate and the high-k dielectric layer; and a deposited oxide layer on the high-k dielectric layer.

2. The integrated circuit as recited in claim 1, wherein the deposited oxide layer is a densified deposited oxide layer.

3. The integrated circuit as recited in claim 2, wherein the high-k dielectric layer is selected from the group consisting of Ta.sub.2 O.sub.5, TiO.sub.2, and **perovskite** materials.

4. The integrated circuit as recited in claim 2, wherein the **perovskite** materials are of the form MTiO.sub.3, where M is selected from the group of Sr, Ba, La, Ti, Pb, Ba.sub.x Sr.sub.1-x and Pb.sub.x La.sub.1-x.

5. The integrated circuit as recited in claim 2, wherein the oxide layers are oxides of silicon.

6. The integrated circuit as recited in claim 5, wherein the silicon substrate is a polysilicon layer.

7. The integrated circuit as recited in claim 5, further comprising a conductive layer on the deposited oxide layer.

8. The integrated circuit as recited in claim 5, wherein the combination of layers forms a gate insulating layer.

9. The integrated circuit as recited in claim 5, wherein the combination of

layers forms a capacitor insulating layer.

10. An integrated circuit having a silicon substrate with a surface, comprising: a grown densified silicon dioxide layer on the silicon substrate surface; a high-k dielectric layer on the grown densified oxide layer, the grown densified oxide layer reducing strain between the silicon substrate and the high-k dielectric layer; and a deposited densified silicon dioxide layer on the high-k dielectric layer.

11. The integrated circuit as recited in claim 10, wherein the high-k dielectric layer is selected from the group consisting of Ta.sub.2 O.sub.5, TiO.sub.2, and **perovskite** materials.

12. The integrated circuit as recited in claim 11, wherein the **perovskite** materials are of the form MTiO.sub.3, where M is selected from the group of Sr, Ba, La, Ti, Pb, Ba.sub.x Sr.sub.1-x and Pb.sub.x La.sub.1-x.

13. The integrated circuit as recited in claim 10, wherein the combination of layers forms a gate insulating layer.

14. The integrated circuit as recited in claim 10, wherein the combination of layers forms a capacitor insulating layer.

15. An integrated circuit having a silicon substrate with a surface, comprising: a densified grown oxide layer on the silicon substrate; no more than one high-k dielectric layer on the grown oxide layer, the grown oxide layer reducing strain between the silicon substrate and the high-k dielectric layer; and a deposited oxide layer on the high-k dielectric layer.

16. The integrated circuit as recited in claim 15, wherein the high-k

dielectric layer is selected from the group consisting of Ta.sub.2 O.sub.4, TiO.sub.2, and **perovskite** materials.

17. The integrated circuit as recited in claim 15, wherein the **perovskite** materials are of the form MTiO.sub.3, where M is selected from the group consisting of Sr, Ba, La, Ti, Pb, Ba.sub.x Sr.sub.1-x and Pb.sub.x La.sub.1-x.

18. The integrated circuit as recited in claim 15, wherein the oxide layers are oxides of silicon.

19. The integrated circuit as recited in claim 15, wherein the silicon substrate is a polysilicon layer.

20. The integrated circuit as recited in claim 15, further comprising a conductive layer on the deposited oxide layer.